Available online at www.sciencedirect.com
ScienceDirect
Microelectronic Engineering 84 (2007) 2901–2906
MICROELECTRONIC ENGINEERING
www.elsevier.com/locate/mee

Lateral SbTeN based multi-layer phase change memory for multi-state storage

You Yin *, Hayato Sone, Sumio Hosaka

Department of Nano-material Systems, Graduate School of Engineering, Gunma University, 1-5-1 Tenjin, Kiryu, Gunma 376-8515, Japan

Received 22 February 2007; accepted 13 March 2007
Available online 18 March 2007

Abstract

X-ray diffraction patterns and resistivity measurement indicate that as-deposited N-doped Sb_2Te_3 (STN) films become amorphous while the as-deposited Sb_2Te_3 film is crystalline. A lateral as-deposited STN-based multi-layer phase change memory was proposed for multi-state storage. The active region of the device consists of a top 30-nm TiN/180-nm STN/20-nm TiN/bottom 120-nm STN stacked multi-layer. Static switching properties of the device with STN initially starting from the amorphous state exhibit two apparent S-shaped switchings, which correspond to two marked device resistance drops by a factor of 2–5. The first and second threshold voltages are around 2.8–3.2 and 4.3–5.4 V, respectively. Finite element analysis of the device shows that the two switchings could sequentially occur at the electrode steps from the bottom 120-nm STN layer to the top thick 180-nm STN layer.

PACS: 81.05Gc; 81.10.Aj; 61.10.Nz

Keywords: N-doped; Sb_2Te_3; Lateral; Phase change memory; Multi-layer; Multi-state

1. Introduction

Phase change memory (PCM) attracted much attention as an emerging nonvolatile memory due to its almost perfect properties such as excellent endurance, non-destructive read, direct overwrite, low programming energy, huge read dynamic range, fast speed, high performance, multi-state storage capability [1–3]. The active chalcogenide phase change (PC) materials in PCMs are characterized by the fast reversible electric-pulse-induced switching between amorphous and crystalline phases, accompanying large differences in electrical properties. The PC layer can locally be poly-crystallized in a PCM through initial filament formation and sequent Joule-heating-induced crystallization processes by applying a long but low electrical pulse and the PCM correspondingly enters a lowly resistive state [4]. On the other hand, it can be amorphized via melting and quenching by applying a short but high electrical pulse so the PCM enters a highly resistive state.

Compared with widely researched $Ge_2Sb_2Te_5$ (GST) chalcogenide, Sb_2Te_3 material for PCM application could have some advantages such as low reset current resulting from its low melting point, and fast crystallization. However, a short retention time is possible for Sb_2Te_3 (ST) material owing to its relatively low crystallization temperature. It is possible to increase its crystallization temperature and thus improve retention time by N-doping into ST (STN) [5,6].

Furthermore, some proposals were put forward to increase the memory capacity of PCM in the past few years. Our group proposed a phase change channel transistor (PCT) which has a build-in reversible-switching chalcogenide resistor and make a 1-transistor memory cell (1 Tr. Cell) feasible [7,8]. And we also proposed some lateral multi-channel PCM for multi-storage. Lai et al. adopted a stacked multi-layer vertical PCM with different chalcogenides (GST and Si-doped GST) [9]. Crystallization pro-

* Corresponding author. Tel.: +81 277 30 1723; fax: +81 277 30 1707.
E-mail address: yinyou@el.gunma-u.ac.jp (Y. Yin).

0167-9317/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2007.03.004

cesses occurred successively in high resistive Si-doped GST and low resistive GST layers, which resulted in three relatively stable resistance states.

Compared with vertical PCMs, lateral PCMs exhibit promising advantages such as low RESET current and power consumption [10–12]. In order to increase capacity of memory and use these advantages, a prototype of a lateral stacked STN-based multi-layer PCM structure is proposed. Resistance drops could result from two sequential switchings from the bottom thin STN layer to the top thick STN layer at the electrode steps. These resistance states induced electrically are stable in a wide voltage window.

2. Experimental methods

200-nm-thick STN film samples with a SiO_2 capping layer on glass substrates were prepared by simultaneously introducing both N_2 and Ar into the chamber using a radio frequency sputtering equipment (MNS-3000-RF, ULVAC, Inc.) at a background pressure below 5×10^{-5} Pa and a sputtering pressure of 0.2 Pa. ST and STN1 (or STN herein) films were prepared at N_2/Ar flow ratios of 0/15 and 1/14 (sccm/sccm), respectively. Systematical study of N-doped ST will be published elsewhere. Crystal structures of films of each kind were characterized by X-ray diffractometer (RINT 2000, Rigaku co.) after annealed on a hot plate from 90 to 290 °C for 5 min. Resistivity as a function of annealing temperature of films was measured by using square-shaped film samples (12×12 mm^2) defined by Ti electrodes.

Current–voltage (I–V) characteristics of the device samples were measured by semiconductor parameter analyzer (4155B, Agilent Technologies, Ltd.). A waveform generator (Model 2571, Tabor Electronics, Ltd.) was adopted to apply single pulses to devices.

3. Experimental results and discussion

3.1. Material properties of ST and STN1 films

X-ray diffraction (XRD) patterns of ST and STN1 films are shown in Fig. 1a and b, respectively. As shown in Fig. 1a, lots of peaks are observed for as-deposited ST film.

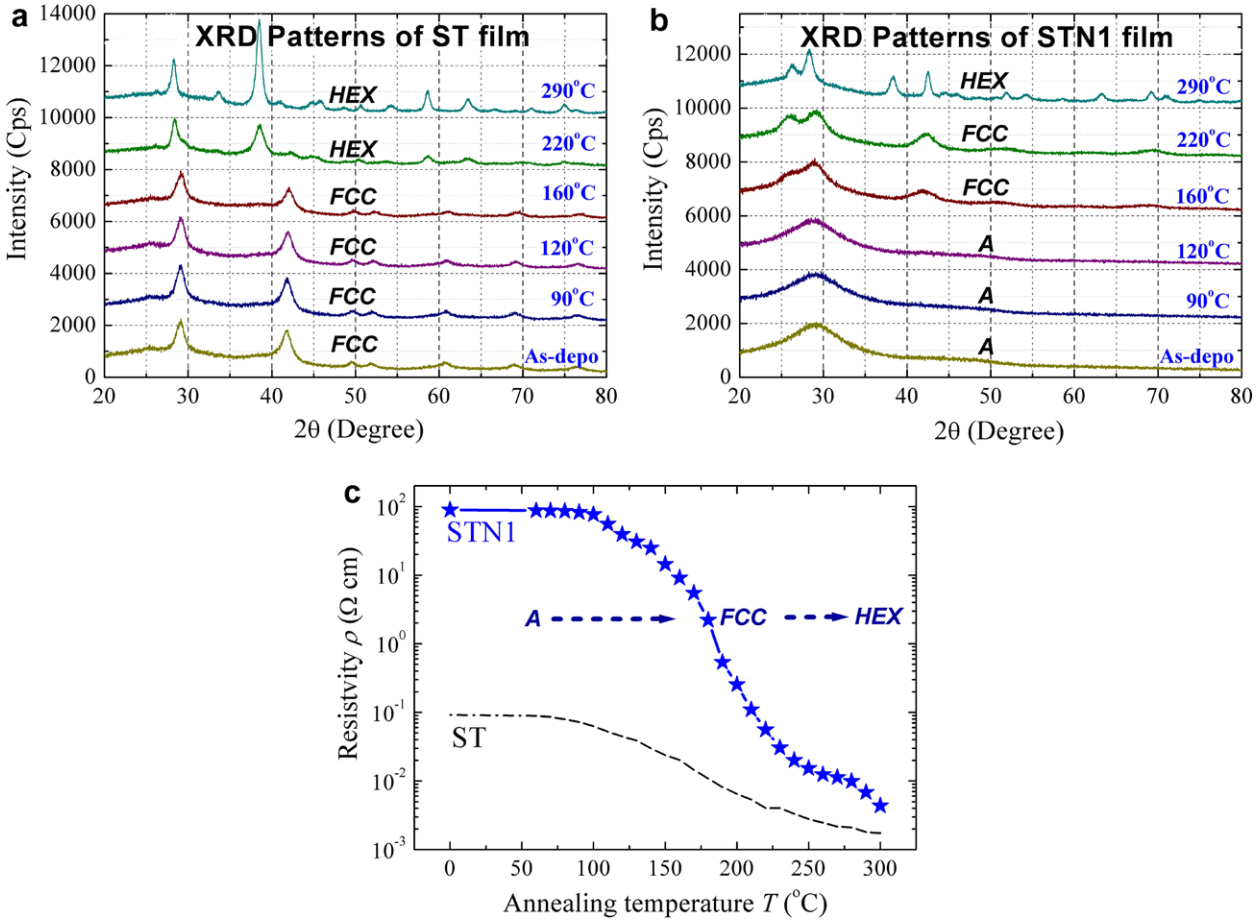

Fig. 1. (a) and (b) X-ray diffraction patterns after annealed at different temperatures up to 290 °C of ST and STN1 films, respectively. (c) Resistivity as a function of annealing temperature of the ST and STN1 films. Phases of STN1 are marked for understanding the relationship between resistivity drop and phase change.

The film is identified to be a face-centered cubic (FCC) crystal structure. The fact that the as-deposited ST film was already crystalline was due to its low crystallization temperature (<100 °C) and increased sample temperature (60–80 °C) during sputtering. The phase transformation of ST films from FCC to a new phase occurred between 160 and 220 °C. The lattice constant a of the FCC crystal structure is determined to be 0.6068 nm on the basis of an analysis of peak positions of the XRD pattern at 160 °C. The new phase is identified to have a hexagonal (HEX) crystal structure according to the XRD pattern at 290 °C. Unlike the ST film, as-deposited STN1 film was amorphous as shown in Fig. 1b. Crystallization to FCC and phase transformation from FCC to HEX occurred in the ranges of 120–160 °C and 220–290 °C, respectively. Therefore, the crystallization temperature from amorphous to FCC ($T_{A\rightarrow F}$) and the phase transformation temperature from FCC to HEX ($T_{F\rightarrow H}$) of the STN1 film are higher than those of ST, respectively.

Fig. 1c shows the relationship between resistivity and annealing temperature up to 300 °C in which thickness reduction due to phase change was neglected. Resistivity of as-deposited ST film was as low as around $9\times10^{-2}\,\Omega$ cm, which resulted from the fact that the as-deposited ST film was already crystalline. Resistivity of the ST film decreased in the range of 100–300 °C. The reduction was due to the phase transformation from FCC to HEX (see XRD patterns in Fig. 1a). On the contrary, resistivity of the as-deposited amorphous STN film is 1000 times of that of the ST film. Crystallization to

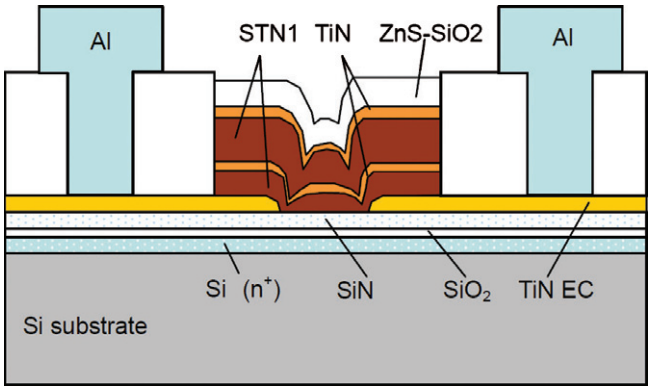

Fig. 2. Schematic diagram of the fabricated lateral as-deposited STN-based multi-layer phase change memory. The active region of the device is composed of a top 30-nm TiN/180-nm STN/20-nm TiN/bottom 120-nm STN stacked multi-layer.

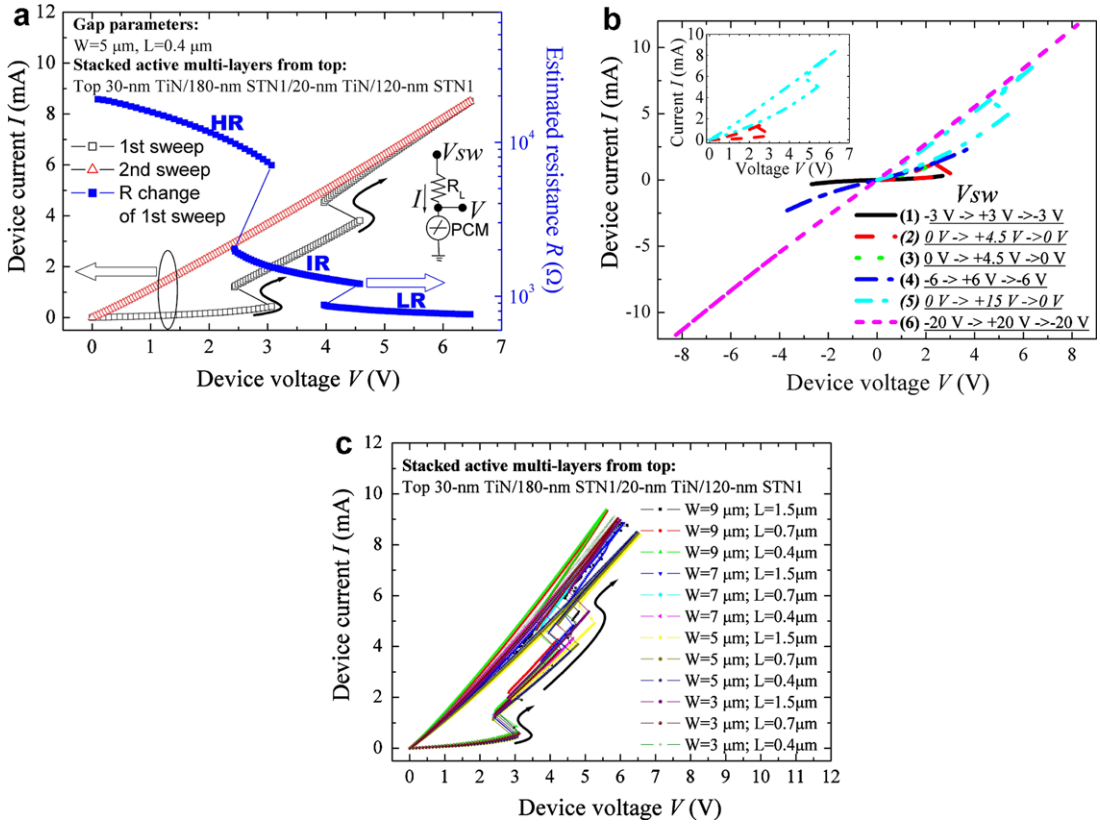

Fig. 3. (a) An example of static switching properties of the fabricated device when V_{sw} was swept to a high sweep voltage. Inset is the circuit used for the measurement. The first sweep from 0 to 15 V exhibits two sudden switchings. The corresponding estimated device resistance indicates two marked drops from HR to IR and then to LR. The second sweep proved that the final state LR was stable. (b) A detailed study of the switching properties with increasing maximum switching voltage by using a device having the same size as that used in (a). (c) Static switching properties of devices with different gap sizes.

FCC led to the marked reduction in resistivity from around 9×10^{1} Ω cm to around 8×10^{-3} Ω cm by about four orders of magnitude. Phase transformation from FCC to HEX resulted in further resistivity drop to around 4×10^{-3} Ω cm of 300 °C.

3.2. STN-based multi-layer PCM device

In order to make use of crystallization to investigate the possibility of multi-state storage and minimize the parasitic current in the switching operations, as-deposited amorphous STN1 films other than as-deposited crystalline ST films were adopted in the devices. The lateral STN-based multi-layer PCM device by using the STN1 PC films was proposed for multi-state storage and schematically shown in Fig. 2. The active region between two lateral TiN electrodes (TiN ECs) consists of a top 30-nm TiN/180-nm STN/20-nm TiN/bottom 120-nm STN stacked multi-layer. The active multi-layer was covered by a 100-nm-thick dielectrics ZnS–SiO_2 capping layer for thermal isolation and device protection. The gap length L between two TiN ECs varies from 0.4 to 3 μm and the width W of the TiN ECs varies from 3 to 9 μm.

3.3. Switching properties of device

Fig. 3 shows an example of static switching properties of the fabricated devices. Inset on the right side of Fig. 3a shows the circuit used for the measurement in which a load resistor R_L of 1 k Ω was used. The PCM device voltage V and current I were measured when we swept the voltage V_{sw} from 0 to 15 V. The first sweep shown as open squares exhibits that two apparent S-shaped switchings occur at threshold voltages of around 3.1 and 4.6 V in terms of the device voltage V, respectively. The curve shown as solid squares illustrates that the estimated device resistance R ($R = V/I$) from the first sweep experienced two sudden drops corresponding to the switchings in the first sweep. The two resistance drops were from high-resistance HR state ('0' state) to intermediate-resistance state LR ('1' state) and from IR to low-resistance state LR ('2' state), respectively. The second sweep shows that the resistance after the second switching was proved stable.

Fig. 3b shows a detailed study of the switching properties with increasing maximum switching voltage by using a device having the same size as that used in Fig. 3a. The initial state HR remained stable at a low voltage sweep as shown in curve (1) in which no switching took place when V_{sw} was swept from −3 to 3 V and then back to −3 V. However, as shown in curve (2), the HR state suddenly changed to the IR state when the device voltage V was a little higher than 3 V when we swept V_{sw} from 0 to 4.5 V and then back to 0 V. The second sweep curve (3) of the same range shows that no further switching took place. Even a higher V_{sw} still did not change the IR state when V_{sw} was swept from −6 to 6 V and then back to −6 V as shown in curve (4). When we swept V_{sw} to a higher voltage, the second switching from IR to LR occurred at a device voltage of around 5.4 V as shown in curve (5). The LR state remained stable at a large sweeping range of V_{sw} from −20 to 20 and then back to −20 V as shown in curve (6). For clearer observation, the two switchings were plotted in inset of Fig. 3b.

As we can see in Fig. 3a and b, two switchings led to two dramatic resistance drops and resulting resistance states (IR and LR) were very stable at a large voltage range. The first switching threshold voltages V_{th1} of the two devices shown in Fig. 3a and b are close, around 3.1 V and the second switching threshold voltages V_{th2} are 4.6 V and 5.4 V, respectively. Fig. 3c shows the I–V plots of PCMs with different gap sizes when the same method as described Fig. 3a, i.e., initially sweeping V_{sw} from 0 to the maximum voltage 15 V, was used for the switching properties measurement. In general, threshold voltage

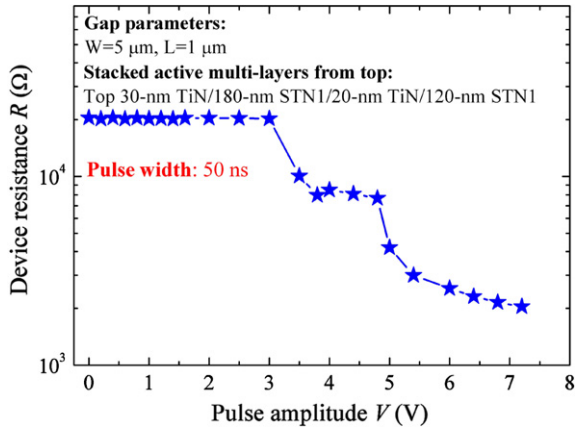

Fig. 4. An example of the pulse-mode dynamic resistance switching behavior with two sudden drops from HR to IR and then to LR by applying 50-ns voltage pulses with increasing pulse amplitude.

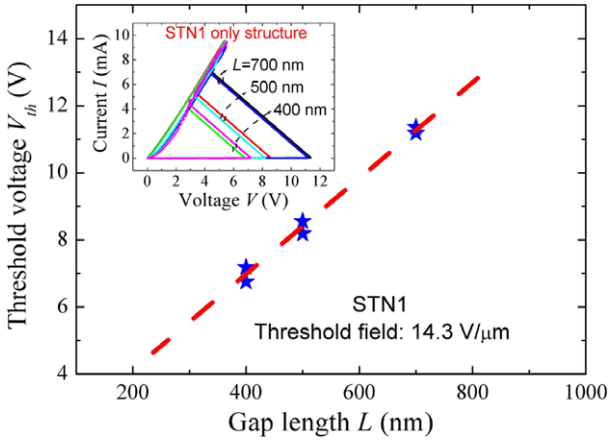

Fig. 5. Threshold field determination for STN1 PC material. Inset shows the switching I–V curves of the PCM device having an only 200-nm-thick STN1 active layer, which were measured by using the same circuit of Fig. 3a.

V_{th2} varies from 4.3–5.4 V. No gap size dependence on V_{th2} could be apparently observed. Thus, it is very likely that the V_{th2} difference between samples of Fig. 3a and b resulted from the device-to-device variation.

Fig. 4 shows an example of the pulse-mode dynamic resistance switching behavior from HR to IR and then to LR by applying 50-ns voltage pulses with increasing pulse amplitude. Device resistance R started from around 20 k Ω and remained stable initially. The first switching occurred when the applied voltage pulse amplitude was above 3 V and then R stayed at a resistance level of around 8 k Ω. The second switching took place at around 5 V and then R gradually decreased to a resistance level of around 2 k Ω. It could be clearly seen in Fig. 4 that the IR state is very stable in the wide pulse amplitude window (3.5–5 V). The LR state was able to be reversibly switched to the HR state by applying a 20-ns voltage pulse with amplitude above 7.5 V. As a result, we demonstrated the possibility of multi-state storage in the STN-based multi-layer PCM device. To optimize switching properties (e.g., reduction in switching threshold voltages, improvement of switching numbers) of the PCM device, those with different PC and barrier materials and layer thicknesses are under investigation.

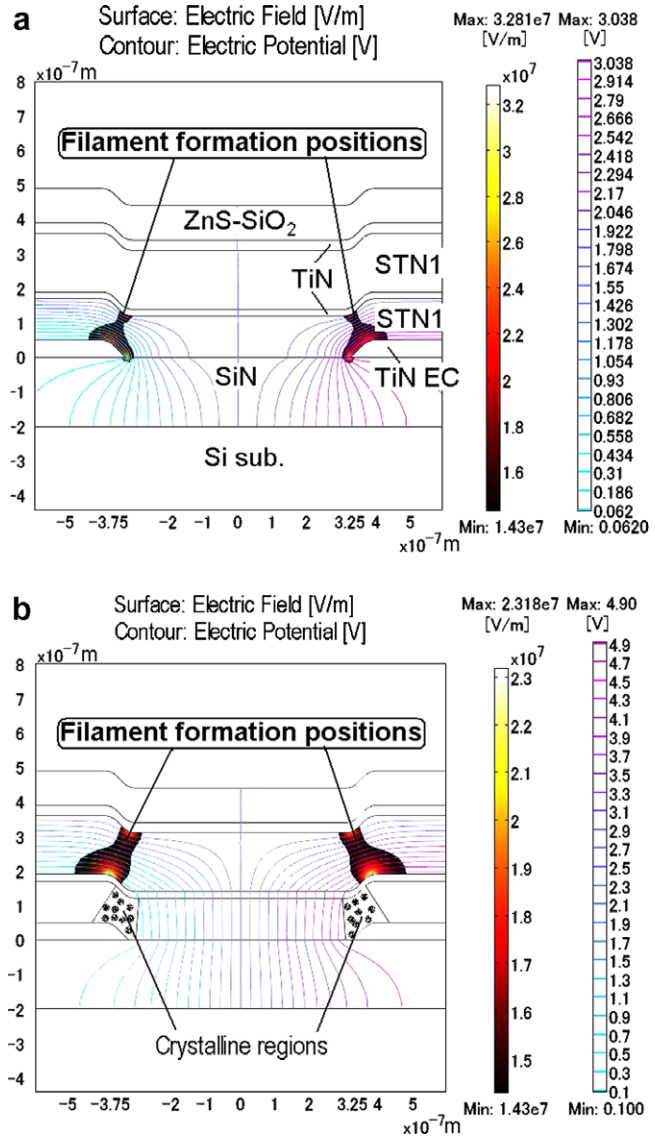

Fig. 6. The FEA simulation results of electric field (shown as surface) and electric potential (shown as contour). Scales are shown in the right side. Filament and crystallization take place in the high electric field regions. (a) The high electric field regions above threshold field 14.3 V/μm are locally defined at the steps of two electrodes edges in the lower STN1 layer when 3.1 V is applied to the amorphous device. (b) The high electric field regions are locally defined in the upper STN1 layer when 5 V is applied to the device in which the lower STN1 layer is already locally crystallized.

4. FEA of fabricated PCM device

Fig. 5 plots the relationship of threshold voltage and gap length of the PCM device having an only 200-nm-thick STN1 active layer instead of aforementioned STN1-based multi-layer. Corresponding threshold field for STN1 PC material was found to be 14.3 V/μm, close to the reported value on the doped-ST by Attenborough [13]. Inset of Fig. 5 shows the switching I–V curves measured using the same circuit of Fig. 3a.

We adopted the commercially available software COMSOL 3.2 for the finite element analysis (FEA) of the PCM device. Fig. 6 shows the simulation results of electric field (as surface) and electric potential (as contour) of a device with a gap length of 0.7 μm. In this model, actual device configuration (such as step coverage and rounded step shape) was taken into account. As shown in Fig. 6a, high electric field regions above threshold field 14.3 V/μm are well defined at the two steps of opposite electrode edges in the lower PC layer when a voltage of 3.1 V is applied to the device electrodes (Ti ECs). Filaments should reasonably forms in the high electric field regions and amorphous-to-crystalline phase transition could take place along these regions. Device resistance correspondingly drops from the HR state to the IR state. After the first resistance drop, a higher voltage of 5 V induces a high electric field distribution as shown in Fig. 6b. Device resistance further reduces from the IR state to the LR state because of filament formation and crystallization at the upper PC layer. The successive phase transitions from lower to upper layers based on electric field could be reasonably used to explain the two resistance drops.

5. Conclusions

A lateral STN-based PCM with a stacked PC multi-layer was proposed for multi-state storage. Both static and dynamic switching of the prototypical device exhibits three stable resistance states (HR, IR and LR). Finite element analysis based on electric field shows that two resistance switchings with increasing applied voltage successively take place at the lower and upper PC layers, respectively.

Acknowledgment

The authors gratefully acknowledge the financial support of the Semiconductor Technology Academic Research Center (STARC) of Japan.

References

[1] S. Lai, T. Lowrey, IEDM Tech. Dig. (2001) 803.
[2] A.L. Lacaita, Solid-State Electron. 50 (2006) 24.
[3] Y. Yin, H. Sone, S. Hosaka, Jpn. J. Appl. Phys. 45 (2006) 8600.
[4] S.R. Ovshinsky, H. Fritzsche, IEEE. Trans. Electron. Dev. 20 (1973) 91.
[5] Y. Yin, N. Higano, K. Ohta, A. Miyachi, M. Asai, A. Miyachi, D. Niida, H. Sone, S. Hosaka, I10.11, San Francisco, CA, USA, 2007 MRS Spring Meeting.
[6] J.H. Oh, S.W. Ryu, B.J. Choi, S. Choi, C.S. Hwang, H.J. Kim, S.Y. Hwang, Y.J. Kim, H.C. Park, H.Y. Chang, S.K. Hong, J. Korean Phys. Soc. 49 (2006) 1173.
[7] S. Hosaka, K. Miyauchi, T. Tumura, Y. Yin, H. Sone, IEEE Trans. Electron. Dev. 54 (2007) 517.
[8] Y. Yin, A. Miyachi, D. Niida, H. Sone, S. Hosaka, Jpn. J. Appl. Phys. 45 (2006) 3238.
[9] Y.F. Cai, Y.Y. Lin, T.A. Tang, B.C. Cai, B. Chen, Appl. Phys. A 84 (2006) 21.
[10] M.H.R. Lankhorst, B.W.S.M.M. Ketelaars, R.A.M. Wolters, Nat. Mater. 4 (2005) 347.
[11] Y. Yin, A. Miyachi, D. Niida, H. Sone, S. Hosaka, Jpn. J. Appl. Phys. 45 (2006) L726.
[12] F. Merget, D.H. Kim, P.H. Bolivar, H. Kurz, Microsyst. Technol. 13 (2007) 169.
[13] K. Attenborough et al., An Alternative Concept for Phase Change Random Access Memory, presented at E*PCOS05.